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☐ 1. Document ID: US 20040056864 A1

Using default format because multiple data bases are involved.

L14: Entry 1 of 19 File: PGPB Mar 25, 2004

PGPUB-DOCUMENT-NUMBER: 20040056864
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040056864 A1

TITLE: Video and graphics system with MPEG specific data transfer commands

PUBLICATION-DATE: March 25, 2004

INVENTOR-INFORMATION:

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US-CL-CURRENT: 345/531

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 2. Document ID: US 20030189571 A1

L14: Entry 2 of 19 File: PGPB Oct 9, 2003

DOCUMENT-IDENTIFIER: US 20030189571 A1
TITLE: Video and graphics system with parallel processing of graphics windows

Detail Description Paragraph:
[0778] In a typical application, graphics data is created by a high-level application tool, e.g., a browser, as individual graphics windows. A lower-level driver for the integrated circuit (IC) chip is typically used to communicate with the IC chip to "load" the graphics windows into a unified memory at external memory location, e.g., the memory 2510 in FIG. 62, so that they may be retrieved to be displayed. Each graphics window is typically treated as an independent object, which may be created and modified by any graphics creation tool.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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3. Document ID: US 20030123219 A1

L14: Entry 3 of 19 File: PGPB Jul 3, 2003

DOCUMENT-IDENTIFIER: US 20030123219 A1
TITLE: Computer backplane with an accelerated graphics port

Detail Description Paragraph:
[0033] The present invention AGP expansion slot fitted with the AGP display card not only allows for high-speed data transfer to the graphics chip, but also can utilizea Unified Memory Architecture (UMA) technology to allow the display card to use a main memory of the computer system as a required graphic memory. It directly uses the main memory to store/access needed information thereby reducing the volumes of used expensive graphics memory.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

4. Document ID: US 20020116576 A1

L14: Entry 4 of 19 File: PGPB Aug 22, 2002

DOCUMENT-IDENTIFIER: US 20020116576 A1
TITLE: System and method for cache sharing

Detail Description Paragraph:
[0028] In one embodiment, when the L2 cache transitions from shared mode to being exclusively accessible by the processor core, a hardware mechanism in the L2 cache changes the state of each of the L2 cache memory locations to be returned to the processor core to invalid. In this way, the processor core will see that the L2 cache memory locations that were released from the graphics engine contain bad or inaccurate data, and the processor core will not attempt to read data from any of these memory locations. This will prevent the processor core from wrongly reading data from a memory location in the L2 cache that had been modified by the graphics engine which, therefore, does not correspond to the data expected by the processor core. In addition, in the flush described regarding block 82, the state of all memory locations in the L2 cache that will be released to the processor core may be set to invalid after they have been flushed.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

5. Document ID: US 6661422 B1

L14: Entry 5 of 19 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6661422 B1
TITLE: Video and graphics system with MPEG specific data transfer commands

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Detailed Description Text (683):
In a typical application, graphics data is created by a high-level application tool, e.g., a browser, as individual graphics windows. A lower-level driver for the integrated circuit (IC) chip is typically used to communicate with the IC chip to "load" the graphics windows into a unified memory at external memory location, e.g., the memory 2510 in FIG. 62, so that they may be retrieved to be displayed. Each graphics window is typically treated as an independent object, which may be created and modified by any graphics creation tool.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 6. Document ID: US 6636222 B1

L14: Entry 6 of 19 File: USPT Oct 21, 2003

DOCUMENT-IDENTIFIER: US 6636222 B1
TITLE: Video and graphics system with an MPEG video decoder for concurrent multi-row decoding

Detailed Description Text (683):
In a typical application, graphics data is created by a high-level application tool, e.g., a browser, as individual graphics windows. A lower-level driver for the integrated circuit (IC) chip is typically used to communicate with the IC chip to "load" the graphics windows into a unified memory at external memory location, e.g., the memory 2510 in FIG. 62, so that they may be retrieved to be displayed. Each graphics window is typically treated as an independent object, which may be created and modified by any graphics creation tool.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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☐ 7. Document ID: US 6573905 B1

L14: Entry 7 of 19 File: USPT Jun 3, 2003

DOCUMENT-IDENTIFIER: US 6573905 B1
TITLE: Video and graphics system with parallel processing of graphics windows

Detailed Description Text (684):
In a typical application, graphics data is created by a high-level application tool, e.g., a browser, as individual graphics windows. A lower-level driver for the integrated circuit (IC) chip is typically used to communicate with the IC chip to "load" the graphics windows into a unified memory at external memory location, e.g., the memory 2510 in FIG. 62, so that they may be retrieved to be displayed. Each graphics window is typically treated as an independent object, which may be created and modified by any graphics creation tool.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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8. Document ID: US 6570573 B1

L14: Entry 8 of 19 File: USPT May 27, 2003

DOCUMENT-IDENTIFIER: US 6570573 B1
** See image for Certificate of Correction **
TITLE: Method and apparatus for pre-fetching vertex buffers in a computer system

Detailed Description Text (14):
Chip set 220 is also coupled to processor bus 210. Chip set 220 may include a memory controller for controlling a main memory 213. In one embodiment, chip set 220 operates according to an Unified Memory Architecture (UMA). Further, chipset 220 may also include an Accelerated Graphics Port (AGP) Specification Revision 2.0 interface developed by Intel Corporation of Santa Clara, Calif. Chip set 220 is coupled to a graphics accelerator 222. According to one embodiment, graphics accelerator 222 process graphics data received at computer system 200.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

9. Document ID: US 6538656 B1

L14: Entry 9 of 19 File: USPT Mar 25, 2003

DOCUMENT-IDENTIFIER: US 6538656 B1
TITLE: Video and graphics system with a data transport processor

Detailed Description Text (684):
In a typical application, graphics data is created by a high-level application tool, e.g., a browser, as individual graphics windows. A lower-level driver for the integrated circuit (IC) chip is typically used to communicate with the IC chip to "load" the graphics windows into a unified memory at external memory location, e.g., the memory 2510 in FIG. 62, so that they may be retrieved to be displayed. Each graphics window is typically treated as an independent object, which may be created and modified by any graphics creation tool.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

10. Document ID: US 6429903 B1

L14: Entry 10 of 19 File: USPT Aug 6, 2002

DOCUMENT-IDENTIFIER: US 6429903 B1
TITLE: Video adapter for supporting at least one television monitor

Detailed Description Text (9):

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The adapter 150 of the preferred embodiment shown in FIG. 2B includes four graphic user interface ("GUI") accelerators 210 although fewer or more could be used. Each accelerator 210 can be coupled to a memory unit 215. The memory units 215 can be synchronous graphic random access memory ("SGRAM") units, although other memory types may be used. The memory units 215 store decoded video data, graphic data from computer operations, character fonts, and other information required for operation of the adapter 150. The shared memory 230 serves as the BIOS for the accelerator card 150. Rather than using two separate BIOS chips for each accelerator, the memory can be shared between the accelerators 210.

☐ 11. Document ID: US 6369824 B1

L14: Entry 11 of 19 File: USPT Apr 9, 2002

DOCUMENT-IDENTIFIER: US 6369824 B1
TITLE: Computer system having an integrated core and graphic controller device capable of accessing memory data simultaneously from a system memory pool and a separate stand-alone frame buffer memory pool

Detailed Description Text (5):
Therefore, the computer system 4 of this invention provides the benefit of more memory access bandwidth associated with 128-bit frame buffer memory data lines for optimizing graphical performance at the lowest memory pin count so that flexibility of system board space/routing can be ensured. Aside from using the same set of address signals to access the memory pools 44, 48 simultaneously during VGA processing, it is noted that most of the control signals during memory access can also be shared by the memory pools 44, 48, thereby further reducing the size of the memory address and control signal bus 49. Furthermore, due to the presence of the VGA-dedicated frame buffer memory pool 48, the impact of a reduction in the size of the system memory pool 44, which is shared by both the core logic and graphic controller portions 421, 422, due to the use of a unified memory architecture can be minimized. As compared with the conventional computer systems of FIGS. 1 to 3, and the computer systems disclosed in the aforesaid co-pending U.S. patent applications, the computer system 4 of the present invention provides more flexibility in system board space/routing than the on-board VGA schemes utilized in the conventional computer systems of FIGS. 1 to 3, and more competitive VGA performance than the computer systems disclosed in the aforesaid co-pending U.S. patent applications. The object of the present invention is thus met.

☐ 12. Document ID: US 6247084 B1

L14: Entry 12 of 19 File: USPT Jun 12, 2001

DOCUMENT-IDENTIFIER: US 6247084 B1
TITLE: Integrated circuit with unified memory system and dual bus architecture

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Detailed Description Text (475):
FIG. 60 is a block diagram of a graphics BitBLT data flow through graphics subsystem 770. The main feature in the graphics subsystem is BitBLT engine 700. BitBLT engine 700 is capable of blitting in either linear address space or in tiled address space due to the tile based frame buffer architecture implemented by memory controller 14. Due to the unified memory architecture of this chip, the frame buffer is connected directly to memory controller 14. All direct rendering and pixel processing by processor 12 is handled in memory controller 14 and not in graphics subsystem 770.

13. Document ID: US 6100936 A

L14: Entry 13 of 19 File: USPT Aug 8, 2000

DOCUMENT-IDENTIFIER: US 6100936 A
TITLE: Multiple-screen video adapter with television tuner

Detailed Description Text (12):
The adapter 150 of the present invention includes two graphic user interface ("GUI") accelerators 210,235. Each accelerator 210,235 is coupled to a memory unit 215,225. The memory units 215,225 are synchronous graphic random access memory ("SGRAM") units, although other memory types may be used. Preferably, each memory unit has a peak memory bandwidth of 800 Megabytes per second (MB/s). The memory units 215,225 store decoded video data, graphic data from computer operations, character fonts, and other information required for operation of the adapter 150. The shared memory 230 serves as the BIOS for the accelerator card 150. Rather than using two separate BIOS chips for each accelerator, the memory is shared between the two accelerators 210,235.

14. Document ID: US 6028643 A

L14: Entry 14 of 19 File: USPT Feb 22, 2000

DOCUMENT-IDENTIFIER: US 6028643 A
TITLE: Multiple-screen video adapter with television tuner

Detailed Description Text (11):
The adapter 150 of the present invention includes two graphic user interface ("GUI") accelerators 210, 235. Each accelerator 210, 235 is coupled to a memory unit 215, 225. The memory units 215, 225 are synchronous graphic random access memory ("SGRAM") units, although other memory types may be used. Preferably, each memory unit has a peak memory bandwidth of 800 Megabytes per second (MB/s). The memory units 215, 225 store decoded video data, graphic data from computer operations, character fonts, and other information required for operation of the

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adapter 150. The shared memory 230 serves as the BIOS for the accelerator card 150. Rather than using two separate BIOS chips for each accelerator, the memory is shared between the two accelerators 210, 235.

☐ 15. Document ID: US 5995121 A

L14: Entry 15 of 19 File: USPT Nov 30, 1999

DOCUMENT-IDENTIFIER: US 5995121 A
TITLE: Multiple graphics pipeline integration with a windowing system through the use of a high speed interconnect to the frame buffer

Detailed Description Text (50):
Accordingly, a method and apparatus for coupling a high performance graphics device to a base graphics subsystem of a workstation has been described. A first pair of interfaces is provided in both the graphics device and the graphics subsystem for transferring data between the graphics device and the graphics subsystem. A second pair of interfaces couples the graphics device directly to a host interface, for transferring commands between the host processor and the graphics device. In one embodiment, all of the interfaces are identically formed, with different portions of the interface being utilized depending upon the location and function of the interface chip. Alternatively, different interfaces also could be provided. The bus structure of the graphics subsystem provides a high speed interconnect to allow one or more external interface chips to be coupled before and accordingly share a common frame buffer. Because the bus structure of graphics subsystem 9 is a ring bus structure, the addition of one or more external graphics devices has minimal impact on the base graphics subsystem performance, yet allows for additional windowing system to be seamlessly integrated with the base graphics system. With such an arrangement, multiple graphics windowing systems may render pixel data to a common frame buffer memory without incurring degrading visual artifacts of the prior art.

☐ 16. Document ID: US 5896140 A

L14: Entry 16 of 19 File: USPT Apr 20, 1999

DOCUMENT-IDENTIFIER: US 5896140 A
** See image for Certificate of Correction **
TITLE: Method and apparatus for simultaneously displaying graphics and video data on a computer display

Brief Summary Text (7):
Display system 10 also includes a video source 20 for inputting a video signal. Video sources such as a video camera, a video cassette recorder, or a television receiver are typically used. The analog video signal from the video source is input

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to an analog-to-digital converter (ADC)/decoder/scaler 24, which converts the analog video signal to a digital signal suitable for use with the other digital components of the system and extracts usable video data and synchronization signals from the digitized video data. The ADC/decoder/scaler 24 outputs digital video data, synchronization signals and other data derived from components well known to those skilled in the art on bus 26, which is mixed with bus 15 output from graphics adapter chip 14. The video data is stored in VRAM 16 and thus shares the memory with graphics data generated by graphics adapter chip 14. Typically, video data is stored in a particular section of memory and is readily accessible by the graphics adapter chip 14. Graphics adapter chip 14 receives information from the microprocessor indicating where the video window is located on the screen and causes graphics data or video data to be output from VRAM 16 when appropriate.

☐ 17. Document ID: US 5883814 A

L14: Entry 17 of 19 File: USPT Mar 16, 1999

DOCUMENT-IDENTIFIER: US 5883814 A
TITLE: System-on-chip layout compilation

Detailed Description Text (66):
FIGS. 10 and 11 show the implementation of global structure and FIG. 13 shows the layout of an integrated logic/DRAM chip for the Unified Media Memory (UMM) application which was designed in 0.25 micron CMOS technology with four layers of metal and device performance enhancement. The UMM chip consists of 64 Mb synchronous DRAM (SDRAM) arranged in eight 8 Mb SDRAM macros. The SDRAM macro supports a synchronous single-bank RAS control, and 1/2/4/8/full page burst modes, to operate at 200 MHz with an I/O width of 64 per macro. The eight SDRAM macros are arranged into two global memory banks for interleaving operation, supplying a wide I/O of 256 bits. The logic functions of the UMM integrated logic/DRAM chip consists of a 256-bit graphic processor (Bit Block Transfer or BitBLT) for manipulating graphic data to/from the SDRAM, a serial access memory (SAM) for exporting the graphic data stream off-chip, a gate-array control unit to generate the control/timing signals for the overall operations of all the macros of the chip, four multiplexer/buffers for high speed import/export of off-chip 64-bit data to the on-chip 256-bit data bus, a phase locked loop (PLL) for generating on-chip clock signals synchronized from an external clock. The macros are communicated through a high bandwidth on-chip 256-bit data bus operating at 133 MHz (200 MHz maximum), a SDRAM address bus, and various control buses such as RAS, CAS, WE, SDRAM enable, and so forth. In addition to the external 64-bit data pins, the chip has 32-bit memory address pins, 32-bit serial data output pins for graphic function, various mode control pins and test pins. it has an interface to the PowerPC.TM. microprocessor bus. The chip can be mounted onto a 240 pin package. The underlying structure of the gate-array random logic macro is also shown in FIG. 13. The DRAM macros perform basic memory function, the logic macros function together with the DRAM macros perform special functions determined by the overall architecture and logic design.

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☐ 18. Document ID: US 5754170 A

L14: Entry 18 of 19 File: USPT May 19, 1998

DOCUMENT-IDENTIFIER: US 5754170 A
TITLE: Transparent blocking of CRT refresh fetches during video overlay using dummy fetches

Detailed Description Text (42):
Graphics pixels are read from graphics memory 56 and written to CRT FIFO 58 during CRT fetches. During dummy fetches pixel data is not read from graphics memory 56 since graphics memory 56 is in use by another requestor such as the host or movie FIFO 30 when movie overlay memory 114 shares the same memory chip as graphics memory 56. However, write counter and decoder 58W is still incremented for all dummy cycles, since the CRT write request signal CRT.sub.-- WR.sub.-- REQ from memory controller 54 is generated when another requester wins arbitration and executes a cycle when dummy.sub.-- CRT is active. Normal CRT FIFO fills activate CRT.sub.-- WR.sub.-- REQ which also increments write counter and decoder 58W. As pixels are shifted out of CRT FIFO 58, even during dummy CRT cycles, CRT.sub.-- WR.sub.-- REQ and CRT.sub.-- RD.sub.-- REQ continue to be generated for dummy cycles during the move envelope.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

☐ 19. Document ID: JP 2004510250 W, WO 200227499 A2, AU 200194840 A, EP 1325417 A2, KR 2003034224 A

L14: Entry 19 of 19 File: DWPI Apr 2, 2004

DERWENT-ACC-NO: 2002-372153
DERWENT-WEEK: 200424

TITLE: Shared translation address caching in memory controller hub using graphics subsystem to perform graphic operations on data and cache to store available locations in memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw De

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Terms	Documents
L12 same graphic$3 near3 data	19

Display Format: - Change Format

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